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| EWULogo.png | | **EAST WEST UNIVERSITY** | |
| **Department of Computer Science and Engineering** | |
| **B.Sc. in Computer Science and Engineering Program** | |
| **Mid Term II Examination, Spring 2018** | |
| **Course:** | | **CSE442 – Microprocessors and Microcontrollers, Section-2** |  |
| **Instructor:** | | **Md. Nawab Yousuf Ali, PhD, Associate Professor, CSE Department** |  |
| **Full Marks:** | | **30 (15 mark will be counted for final grading)** |  |
| **Time:** | | **1 Hour and 20 Minutes** |  |
| **Note:** There are EIGHT questions, answer ALL of them. Course outcomes (CO), cognitive levels and marks of each question are mentioned at the right margin. | | | |
| 1. | Determine the activities of the following pins in 8086 microprocessor when   1. INTR is logic 1 2. TEST is logic 0 3. ALE is logic 1 | | [CO1, C3, 3] |
| 2. | Determine the output of the following table during bus cycle status of 8088 microprocessor using   |  |  |  |  | | --- | --- | --- | --- | |  |  |  | Output | | 0 | 0 | 0 |  | | 0 | 1 | 0 |  | | 1 | 0 | 0 |  | | 0 | 0 | 1 |  | | 0 | 1 | 1 |  | | 1 | 0 | 1 |  | | 1 | 1 | 0 |  | | 1 | 1 | 1 |  | | | [ CO1, C4, 4] |
| 3. | Define the addresses, data and control inputs, latches and status pins in the following bus buffering of 8086 microprocessor. | | [ CO1, C3, 3] |
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| 4. | Design an interface between a memory 27128 EPROM and Intel 8086 microprocessor using a NAND gate. Calculate the memory location for the EPROM. Explain very briefly. | | [CO2, C3, 6 ] |
| 5 | Design an address multiplexer for DRAM that contains only 16 address inputs, where it should contain 32-the numbered required addressing 4GB memory locations. Determines the pins functions for the operations. | | [ CO2, C3, 5 ] |
| 6 | Consider a software interrupt with BOUND instruction.  Write the outputs for the conditions in the box.  if (AX<(DATA+(DATA+1))) ; DATA is a one byte of a memory location  if (AX>((DATA+2) +(DATA+3))) | | [ CO2, C3, 3] |
| 7. | Determine the type and memory addresses for the following interrupt vectors.   1. Double fault 2. Undefined opcode 3. Page fault | | [CO2, C3, 3] |
| 7. | Design a circuit that applies an interrupt vector type number 4 in response to. | | [CO2, C3, 3] |

*\*\*\*GOOD LUCK\*\*\**